What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming an interconnect structure, said method comprising the steps of:

forming a second opening through a second insulating layer which is provided over a first insulating layer, said first and second insulating layers comprising a low dielectric constant material;

time etching a first opening through said first insulating layer, said first opening being in communication with said second opening; and

providing a first conductive material in said first and second openings.

2. The method of claim 1, wherein said first insulating layer id formed of organic material.

3. The method of claim 2, wherein said organic material is selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene and SILK.

4. The method of claim 2, wherein said first insulating layer is formed of SILK.

5. The method of claim 1, wherein said first insulating layer is formed of a low dielectric constant inorganic material.

6. The method of claim 5, wherein said inorganic material is selected from the group consisting of fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

7. The method of claim 5, wherein said first insulating layer is formed of NANOGLASS.

8. The method of claim 1, wherein said first insulating layer is formed by deposition to a thickness of about 4,000 to 30,000 Angstroms.

9. The method of claim 8, wherein said first insulating layer is formed by deposition to a thickness of about 12,000 to 20,000 Angstroms.

10. The method of claim 1, wherein said second insulating layer is formed of a low dielectric constant organic material.

11. The method of claim 10, wherein said low dielectric constant organic material selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene and SILK.

12. The method of claim 10, wherein said second insulating layer is formed of SILK.

13. The method of claim 1, wherein said second insulating layer comprises a low dielectric constant inorganic material.

14. The method of claim 13, wherein said inorganic material is selected from the group consisting of fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

15. The method of claim 13, wherein said second insulating layer is formed of NANOGLASS.

16. The method of claim 1, wherein said second insulating layer is formed by deposition to a thickness of about 1,000 to 2,000 Angstroms.

17. The method of claim 16, wherein said second insulating layer is formed by deposition to a thickness of about 500 Angstroms.

18. The method of claim 1, wherein said first and second insulating layers are formed of different materials which can be selectively etched relative to each other.

19. The method of claim 18, wherein said step of forming said first opening is achieved by time etching said first insulating layer with a first etch chemistry.

20. The method of claim 19, wherein said step of forming said second opening is achieved by etching said second insulating layer with a second etch chemistry.

21. The method of claim 1, wherein said first conductive material is blanket deposited.

22. The method of claim 1, wherein said first conductive material is formed of a material selected from the group consisting of copper, copper alloy, gold, gold alloy, silver, silver alloy, tungsten, tungsten alloy, aluminum, and aluminum alloy.

23. The method of claim 1 further comprising the step of chemical mechanical polishing said first conductive material.

24. The method of claim 1 further comprising the step of forming a barrier layer before said step of providing said first conductive material.

25. The method of claim 1 further comprising the steps of:

forming a fourth opening through a fourth insulating layer which is provided over a third insulating layer, said third insulating layer being formed over said conductive material, said third and fourth insulating layers comprising a low dielectric constant material;

time etching a third opening through said third insulating layer, said third opening being in communication with said fourth opening; and

providing a second conductive material in said third and fourth openings.

26. The method of claim 25, wherein said third insulating layer is formed of organic material.

27. The method of claim 26, wherein said organic material is selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene and SILK.

28. The method of claim 26, wherein said third insulating layer is formed of SILK.

29. The method of claim 25, wherein said third insulating layer is formed of a low dielectric constant inorganic material.

30. The method of claim 29, wherein said inorganic material is selected from the group consisting of fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

31. The method of claim 29, wherein said third insulating layer is formed of NANOGLASS.

32. The method of claim 25, wherein said third insulating layer is formed by deposition to a thickness of about 4,000 to 30,000 Angstroms.

33. The method of claim 32, wherein said third insulating layer is formed by deposition to a thickness of about 12,000 to 20,000 Angstroms.

34. The method of claim 25, wherein said fourth insulating layer is formed of a low dielectric constant organic material.

35. The method of claim 34, wherein said low dielectric constant organic material is selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene and SILK.

36. The method of claim 35, wherein said fourth insulating layer is formed of SILK.

37. The method of claim 25, wherein said fourth insulating layer is formed of a low dielectric constant inorganic material.

38. The method of claim 37, wherein said inorganic material is selected from the group consisting of fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

39. The method of claim 37, wherein said fourth insulating layer is formed of NANOGLASS.

40. The method of claim 25, wherein said fourth insulating layer is formed by deposition to a thickness of about 1,000 to 2,000 Angstroms.

41. The method of claim 40, wherein said fourth insulating layer is formed by deposition to a thickness of about 500 Angstroms.

42. The method of claim 25, wherein said third and fourth insulating layers are formed of different materials which can be selectively etched relative to each other.

43. The method of claim 42, wherein said step of forming said third opening is achieved by time etching said third insulating layer with said second etch chemistry.

44. The method of claim 43, wherein said step of forming said fourth opening is achieved by etching said second insulating layer with said first etch chemistry.

45. The method of claim 25, wherein said second conductive material is blanket deposited.

46. The method of claim 25, wherein said second conductive material is formed of a material selected from the group consisting of copper, copper alloy, gold, gold alloy, silver, silver alloy, tungsten, tungsten alloy, aluminum, and aluminum alloy.

47. The method of claim 25 further comprising the step of chemical mechanical polishing said second conductive material.

48. The method of claim 25 further comprising the step of forming a barrier layer before said step of providing said second conductive material.

49. A method of forming a damascene interconnect structure, said method comprising the steps of:

forming a first SILK layer over at least a portion of a metal layer provided within a substrate;

forming a first NANOGLASS layer over said first SILK layer;

forming a second opening within said first NANOGLASS layer;

forming a first opening within said first SILK layer and extending said first opening to said metal layer;

providing a first conductive material in said first and second openings;

forming a second NANOGLASS layer in contact with said first conductive material;

forming a second SILK layer over said second NANOGLASS layer;

forming a fourth opening within said second SILK layer;

forming a third opening within said second NANOGLASS layer and extending said third opening to said first conductive material; and

providing a second conductive material in said third and fourth openings.

50. The method of claim 49, wherein said step of forming said first opening is achieved by time etching said first SILK layer with a first etch chemistry.

51. The method of claim 50, wherein said step of forming said fourth opening is achieved by etching said second SILK layer with said first etch chemistry.

52. The method of claim 49, wherein said step of forming said third opening is achieved by time etching said second NANOGLASS layer with a second etch chemistry.

53. The method of claim 52, wherein said step of forming said second opening is achieved by etching said first NANOGLASS layer with said second etch chemistry.

54. The method of claim 53, wherein said first etch chemistry is an oxygen plasma chemistry and said second etch chemistry is a chlorine plasma chemistry.

55. The method of claim 49, wherein each of said first SILK layer and said second NANOGLASS layer is formed by deposition to a thickness of about 4,000 to 30,000 Angstroms.

56. The method of claim 55, wherein each of said first SILK layer and said second NANOGLASS layer is formed by deposition to a thickness of about 12,000 to 20,000 Angstroms.

57. The method of claim 49, wherein each of said first NANOGLASS layer and said second SILK layer is formed by deposition to a thickness of about 1,000 to 2,000 Angstroms.

58. The method of claim 57, wherein each of said first NANOGLASS layer and said second SILK layer is formed by deposition to a thickness of about 500 Angstroms.

59. An integrated circuit structure, comprising:

a first and second insulating layers with a dielectric constant lower than 4.0 provided over a semiconductor substrate and contacting at least a portion of a metal layer provided within said semiconductor substrate;

at least a first opening within said first and second insulating layers, said first opening being formed by time etching of at least one of said first and second insulating layers with a first etch chemistry;

a third and fourth insulating layers with a dielectric constant lower than 4.0 provided over said second insulating layer; and

at least a second opening within said third and fourth insulating layers, said second opening being formed by time etching of at least one of said third and fourth insulating layers with a second etch chemistry.

60. The integrated circuit structure of claim 59, wherein said first and second insulating layers comprise organic material.

61. The integrated circuit structure of claim 60, wherein said organic material is selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene and SILK.

62. The integrated circuit structure of claim 59, wherein said first insulating layer comprises SILK material and said second insulating layer comprises NANOGLASS material.

63. The integrated circuit structure of claim 59, wherein said first and second insulating layers comprise inorganic material.

64. The integrated circuit structure of claim 63, wherein said inorganic material is selected from the group consisting of fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

65. The integrated circuit structure of claim 59, wherein said third and fourth insulating layers comprise organic material.

66. The integrated circuit structure of claim 65, wherein said organic material is selected from the group consisting of polyimide, spin-on-polymers, flare, polyarylethers, parylene, polytetrafluoroethylene, benzocyclobutene and SILK.

67. The integrated circuit structure of claim 59, wherein said fourth insulating layer comprises SILK material and said third insulating layer comprises NANOGLASS material.

68. The integrated circuit structure of claim 59, wherein said third and fourth insulating layers comprise inorganic material.

69. The integrated circuit structure of claim 68, wherein said inorganic material is selected from the group consisting of fluorinated silicon oxide, hydrogen silsesquioxane and NANOGLASS.

70. The integrated circuit structure of claim 59, wherein said first and second insulating layers are formed of different materials which can be selectively etched relative to each other.

71. The integrated circuit structure of claim 70, wherein said third and fourth insulating layers are formed of different materials which can be selectively etched relative to each other.

72. A processor-based system, comprising:

a processor; and

an integrated circuit coupled to said processor, at least one of said processor and integrated circuit including an interconnect structure, said interconnect structure comprising a first and second insulating layers with a dielectric constant lower than 4.0

provided over a semiconductor substrate and contacting at least a portion of a metal layer provided within said semiconductor substrate; at least a first opening within said first and second insulating layers, said first opening being formed by time etching of at least one of said first and second insulating layers with a first etch chemistry; a third and fourth insulating layers with a dielectric constant lower than 4.0 provided over said second insulating layer; and at least a second opening within said third and fourth insulating layers, said second opening being formed by time etching of at least one of said third and fourth insulating layers with a second etch chemistry.

73. A damascene interconnect structure on a semiconductor substrate, comprising:

a first plurality of first and second insulating layers with a dielectric constant lower than 4.0 provided over a semiconductor substrate and contacting at least a portion of a metal layer provided within said semiconductor substrate;

at least a first via within said first plurality, said first via being formed by time etching of at least one of said first and second insulating layers with a first etch chemistry;

a second plurality of third and fourth insulating layers with a dielectric constant lower than 4.0 provided over said second insulating layer; and

at least a second via within said second plurality, said second via being formed by time etching of at least one of said third and fourth insulating layers with a second etch chemistry.

74. The damascene interconnect structure of claim 73 further comprising a third plurality of fifth and sixth insulating layers with a dielectric constant lower than 4.0 provided over said fourth insulating layer.

75. The damascene interconnect structure of claim 74 further comprising at least a third via within said third plurality, said third via being formed by time etching of at least one of said fifth and sixth insulating layers with said first etch chemistry.